

ESD Circuits, ESD Standards Overview for the Device Testing Technologist Latch-up Physics & Design, Impact of CMOS Scaling on ESD HCPH

Offered by the ESD Association

Date: July 14-15, 2008 • Lunch and refreshments provided
The AMD Commons Bldg, One AMD Place, Sunnyvale, CA

DEVICE TECHNOLOGIST

▲ ESD Circuits*

July 14, 2008, 8:30 a.m. - 4:30 p.m.

Instructors: Timothy J. Maloney, *Intel Corporation*; Steven H. Voldman, *Steven H. Voldman LLC*;
Eugene Worley, *Chronicle Technology, Inc.*

A full-day course is provided with the focus solely on on-chip electrostatic discharge (ESD) protection networks, and circuits for digital, analog and RF circuits. The course will emphasize ESD input networks, and ESD power clamps providing many examples of both diode, MOSFET and bipolar transistor based solutions. The course will focus on fundamental concepts of ESD circuit design practices, design synthesis, diode and MOSFET design, I/O networks (receivers and off-chip drivers), ESD input circuits, and ESD power clamps. The course will add special topics such as ESD power clamp optimization, cross-power domain issues, SOI, to RF application issues.

▲ ESD Standards Overview for the Device Testing Technologist*

July 15, 2008, 8:30 a.m. - Noon

Instructor: Leo G. Henry, *ESD-TLP Consultants*

The ESD Association introduction of the Device Design Certification curriculum has created a need for additional classes that will help with the understanding of some of the technical material presented in the actual DD curriculum. Not all aspects of the existing Device Test (DT) standards are covered in tutorials. This new DT tutorial provides an overview of the Device Testing Standards (S), Standard Test Methods (STM) and Standard Practice (SP) documents. The existing DT –HBM, MM, CDM, TLP Component level class covers why the testing is done, and explains the technical differences between the ESD models. This new class will cover overall requirements, specifications, equipment calibration, verification and qualification for the above DT models. The course will also cover the testing setup, testing procedures, testing requirements and the proper application indicated in each of the DT documents.

*These are NOT DD certification courses

DEVICE DESIGN

▲ Latch-up Physics & Design

July 15, 2008, 1:00 p.m. - 2:30 p.m.

Instructor: Steven H. Voldman, *Steven H. Voldman LLC*

Latch-up continues to be of interest today in advanced CMOS, mixed signal (MS) CMOS, RF, CMOS, BiCMOS, and BiCMOS silicon germanium. The latch-up tutorial will provide a discussion on device-level latch-up physics, latch-up metric and design criteria, latch-up test structures, test methods, latch-up measurement techniques, device-level AZD simulation, and new latch-up issues. Both internal and external latch-up phenomena, as well as DC and transient latch-up will be addressed. Latch-up structures, guard ring physics, and characterization will be discussed in depth. The tutorial will provide examples of discussion on latch-up device level simulation using latch-up scaling issues as examples. Latch-up process solutions, such as heavily doped buried layers (HDBL) and triple wells will be shown. The tutorial will briefly discuss latch-up standards. The tutorial will end with a discussion on the state-of-the-art latch-up issues and characterization techniques and tools.

▲ Impact of CMOS Technology Scaling on ESD HCPH

July 15, 2008, 3:00 p.m. - 4:30 p.m.

Instructor: Steven H. Voldman, *Steven H. Voldman LLC*

This advanced tutorial will cover the impact of silicon technology scaling on ESD device behavior and on subsequent ESD protection design. The physics of CMOS components under high current conditions will be discussed. Also, the technology trends for sub-100nm nodes and their implications for the ESD design window will be covered. Finally, sub-50nm technologies challenges will be discussed. This class is intended for individuals who have taken the basic on-chip protection class and are familiar with basic device physics for both ESD and latch-up.

Device Design

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About the Instructors

Steven H. Voldman is an IEEE Fellow for "Contributions in ESD protection in CMOS, Silicon On Insulator and Silicon Germanium Technology." In the ESD Association, Voldman initiated the "ESD on Campus" program which was established to bring ESD lectures and interaction to university faculty and students internationally; the ESD on Campus program has reached over 24 universities in the United States, Singapore, Taiwan, Malaysia, Philippines, Thailand, and China. Dr. Voldman has written over 150 technical papers between 1982 and 2007. He is a recipient of over 164 issued US patents and 91 US patents pending, in the area of ESD and CMOS latch-up. Dr. Voldman also has written an article for Scientific American in October 2002. Dr. Voldman has authored four books: *ESD: Physics and Devices*; *ESD: Circuits and Devices*; *ESD: Radio Frequency (RF) Technology and Circuits*; and a new release, *Latch-up*.

Eugene Worley received the MSEE degree from the University of California at Berkeley in Solid State Electronics. His career has included IC circuit design, semiconductor device characterization, and reliability physics on various technologies such as CMOS, CMOS/SOS, Flash Non Volatile Memory, SiGe bipolar, and GaAs. He is presently a principle engineer at Qualcomm and has been a member of the ESDA since 1991. His work at Qualcomm has included designing ESD protection devices for PMIC, RF, and USB circuits. For over 3 years Mr. Worley was an industry consultant through his company, Silicon Crossing. He has developed ESD clamps for technologies as diverse as 20 and 100V MOSFETs and Serdes I/O as well as standard CMOS circuits ranging from 0.8 μ m down to 32nm. His ESDA activities have included being a member of the TLP Standards Committee, workshop moderator for 3 years, workshop panelist for 6 years, session chair for 4 years and Technical Program Committee member for 9 years. He has published papers in the IEEE Transactions on Electron Devices, IEEE Electron Device Letters, IEEE J. of Solid State Circuits, Solid State Electronics, the Technical Digest of the International Electron Devices Meeting, the EOS/ESD Symposium Proceedings, Journal of Electrostatics, and the IEEE Transactions on Nuclear Science. He has also reviewed papers for the IEEE Transactions on Electron Devices and Transactions on Device and Materials Reliability. He is a member of Tau Beta Pi, Eta Kappa Nu, and Phi Kappa Phi.

Timothy J. Maloney received an S.B. degree in Physics from the Massachusetts Institute of Technology in 1971, an M.S. in Physics from Cornell University in 1973, and a Ph.D. in Electrical Engineering from Cornell in 1976, where he was a National Science Foundation Fellow. He was a Postdoctoral Associate at Cornell until 1977, when he joined the Central Research Laboratory of Varian Associates, Palo Alto, CA. At Varian until 1984, he worked on III-V semiconductor photocathodes, solar cells and microwave devices, as well as silicon molecular beam epitaxy and MOS process technology. Since 1984 he has been with Intel Corporation, Santa Clara, CA, where he has been concerned with integrated circuit ESD protection, CMOS latch-up testing, fab process reliability, signal integrity, and design and testing of standard IC layouts. He is now a Senior Principal Engineer at Intel. He has received the Intel Achievement Award for his patented ESD protection devices, which have achieved breakthrough ESD performance enhancements for a wide variety of Intel products. He now holds 28 patents, with several more pending. Dr. Maloney received Best Paper Awards for his contributions to the EOS/ESD Symposium in 1986 and 1990, was General Chairman for the 1992 EOS/ESD Symposium, and received the ESD Association's Outstanding Contributions Award in 1995. He has taught short courses at UCLA, University of Wisconsin, and UC Berkeley. He is coauthor of the book, "Basic ESD and I/O Design" (Wiley, 1998), and is a Senior Member of the IEEE.

Leo G. Henry is presently an Electrostatic Discharge (ESD) consulting engineer. He has worked in the electronics industry for almost 25 years and in the field of Electrical Overstress (EOS) and ESD for over 18 years. Over the years, Leo G. has worked in several engineering capacities for several companies and had previously spent over 14 years at Advanced Micro Devices (AMD) as a Member of the Engineering Technical Staff (MTS). Leo G. received his B.Sc. and M.Sc. degrees in Physics from the University of the West Indies. He received his M.S. and Ph.D. degrees in Materials Science at the University of California at Berkeley. Dr. Henry has taught Physics at the University of West Indies, Materials Science and Failure Analysis Principles at San Jose State University and ESD at various Conferences. He has tutored ESD at most of the ESDDiscovery seminars, taught EOS/ESD Failure Analysis and IC ESD Testing at the EOS/ESD Symposium (1997-2007) and also at ASM's ISTFA (1997-2007). Dr. Henry has presented at conferences and published many papers on ESD, EOS, Transmission Line Pulsing (TLP), Failure Signature Analysis and Materials Science. His technical expertise also includes system level testing using the IEC ESD standard. Dr. Henry is a senior member of the IEEE, a member of ASM/EDFAS and BoD member of SiVa, the Silicon Valley EOS/ESD society. Leo G. is presently overall chair of the ESD Association's ESD Device Testing Standards WG-5.0, and chair of the Charged Device Model (CDM) WG-5.3.1. He has served on the ESDA's ESD Symposium Technical Program Committee (1996-2006), as National Tutorial Program (NTP) chair (2003-2006), and is a member of the Association's Technical and Administrative Support (TAS) Committee for Standards. As an elected member (1995-2000 & 2002-2008) of the Board of Directors of the ESDA, he is part of the industry liaison team, and is presently the Vice President of the ESD Association.

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Registration Form

Last Name: _____ First Name: _____

Company Name: _____

Street: _____ City: _____

State/Province: _____ Country _____ Zip/Postal Code: _____

Is Address (please circle the one that applies) Home or Company

Phone: _____ Fax: _____ Email: _____

Course Selection

July, 14, 2008

ESD Circuits (8:30 a.m. - 4:30 p.m.)

July, 15, 2008

ESD Standards Overview for the Device Testing Technologist (8:30 a.m. - Noon)

Latch-up Physics & Design (1:00 p.m. - 2:30 p.m.)

Impact of CMOS Technology Scaling on ESD HCPH (3:00 p.m. - 4:30 p.m.)

	Cost on or before 5/9/08		Cost after 5/9/08	
	Members	Non-Members	Members	Non-Members
1/2 day - each (AM session or both PM sessions)	\$295	\$395	\$495	\$495
Full Day (1 day or two half days)	\$495	\$595	\$695	\$695
Both Full Days	\$990	\$1,190	\$1,390	\$1,390

Payment Information

Payment is required at time of registration. Only checks drawn in U.S. currency on a U.S. bank that is a member of the Federal Reserve will be accepted; make checks payable to ESD Association. Visa®, Mastercard®, and American Express® are accepted.

Amount enclosed \$ _____ Check Credit Card

Credit card type: Visa® Mastercard® American Express®

Credit card number: _____ Security code: _____

Name on card: _____ Expiration date: _____

Cardholder's signature: _____

Accommodations

Walking Distance
Residence Inn – Silicon Valley II
1080 Stewart Drive, Sunnyvale, CA
(408) 720-8893

Nearby
Four Points Sheraton – Sunnyvale
1250 Lakeside Dr, Sunnyvale, CA
(408) 738-4888

Please Email, Fax or Mail completed form to:

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